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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/574,066	03/30/2006	Theodore J. Letavic	US03 0376 US2	9392
65913 NXP, B.V. NXP INTELLECTUAL PROPERTY & LICENSING M/S41-SJ 1109 MCKAY DRIVE SAN JOSE, CA 95131	7550 06/12/2009		<div>EXAMINER</div> <div>GEBREMARIAM, SAMUEL A</div>	
			<div>ART UNIT</div> <div>2811</div>	<div>PAPER NUMBER</div>
			<div>NOTIFICATION DATE</div> <div>06/12/2009</div>	<div>DELIVERY MODE</div> <div>ELECTRONIC</div>

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary

Application No.

10/574,066

Applicant(s)

LETAVIC, THEODORE J.

Examiner

SAMUEL A. GEBREMARIAM

Art Unit

2811

Period for Reply -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 March 2009.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-31 is/are pending in the application.
- 4a) Of the above claim(s) 6-21 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5 and 21-31 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-8508)
- Paper No(s)/Mail Date _____

- 4) ☐ Interview Summary (PTO-413)
- Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-5 and 22-31 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The figure does not clearly describe the elements of the bipolar device. Although it is well known that MOS device has a parasitic bipolar transistor, it is not clear from the description as to the exact location of the emitter, base and collector of the bipolar device.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-5 and 22-31 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is not clear what the structural relationship is between the trench gate, source, body, and drain of the MOS device and the emitter, base and collector region and the

bipolar device. Where the emitter, base and collector of the bipolar device in relation to MOS device?

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1-5 and 29-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Warwick, US 2001/0023957.

Regarding claims 1 and 29-31, as best the examiner is able to ascertain the claimed invention, Warwick teaches a hybrid MOS-bipolar device comprising a trench MOS device having a source (13A), gate (21), where the gate (21) is a trench gate, drain (14) and body regions (15A). Since Warwick teaches a MOS device and since a MOS transistor has a parasitic bipolar transistor, Warwick teaches an emitter, a collector and base.

Warwick does not explicitly state that the gate and the body being shorted together and biased positively relative to the drain.

However shorting a gate and a body region is conventional and well known that is routinely practice to use transistors as a breakdown diodes.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to short the body and the gate as claimed in the structure of Warwick, in order to use the MOS device as a breakdown diode.

Regarding claim 2, Warwick teaches substantially the entire claimed structure of claim 1 above except explicitly stating that a gate oxide having has a single oxide thickness of under 600Å.

Parameters such as oxide thickness in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device characteristics during fabrication.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the oxide thickness as claimed in the structure of Warwick, in order to use the MOS device as a breakdown diode.

Regarding claim 3, Warwick teaches substantially the entire claimed structure of claim 1 above including a gate oxide having multiple oxide thicknesses for formation of gate and field-oxide regions (Warwick teaches device isolation regions).

Regarding claim 4, Warwick teaches substantially the entire claimed structure of claim 1 above including a square trench geometry (figs. 6 and 7).

Regarding claim 5, Warwick teaches substantially the entire claimed structure of claim 1 above including the trench gate having a circular geometry (circular trench gates are well known).

Regarding claims 22-27, as best the examiner is able to ascertain the claimed invention, Warwick teaches a hybrid MOS-bipolar device comprising: a MOS device

having a trench gate (21), a source (13a), a drain (14) and a body (15); a bipolar device having an emitter, a collector, a base and a gate formed by the trench gate, the emitter and the source being formed by a common region (Warwick teaches a MOS device and since a MOS transistor has a parasitic bipolar transistor, Warwick teaches an emitter, a collector and base), the base and the body being formed by a common region, and the collector and the drain being formed by a common region; a substrate that includes a PI region and an N drift region, the trench gate extending from a top surface of the substrate through the PI region into the N drift region; a first electrode coupled to the trench gate, the body and the base; and a second electrode coupled to the source and the emitter.

Warwick does not explicitly state that the gate and the body being shorted together and biased positively relative to the drain.

However shorting a gate and a body region is conventional and well known that is routinely practice to use transistors as a breakdown diodes.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to short the body and the gate as claimed in the structure of Warwick, in order to use the MOS device as a breakdown diode.

Response to Arguments

7. Applicant's arguments with respect to claims 1-5 and 22-31 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel A Gebremariam whose telephone number is (571) 272-1653. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on (571) 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/SAG/

June 8, 2009

/Samuel A Gebremariam/

Examiner, Art Unit 2811